Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6225207").PN.	US-PGPUB; USPAT	OR	OFF	2004/12/15 14:52
L2	536	(triple or third) with (hard adj mask)	US-PGPUB; USPAT	OR	ON	2004/12/15 15:30
L3	498	2 and (hole or opening or recess or aperture or trench or via)	US-PGPUB; USPAT	OR	ON	2004/12/15 15:30
L4	364	3 and @ad<"20020930"	US-PGPUB; USPAT	OR	ON	2004/12/15 14:55
L5	87	(triple or third) with (hard adj mask)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/15 15:30
L6	51	5 and (hole or opening or recess or aperture or trench or via)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/15 15:31

	U	1 [1]	Document ID	Issue Date	Pages	Title
1		X	US 20030139034 A1	20030724	13	Dual damascene structure and method of making same
2		X	US 20030119307 A1	20030626	15	Method of forming a dual damascene structure
3		X	US 20030044725 A1	20030306	23	Dual damascene process using metal hard mask
4		X	US 6514852 B2	20030204	29	Semiconductor device and method of manufacturing the same
5		X	US 6514671 B1	20030204	16	Interconnect line formed by dual damascene using dielectric layers having dissimilar etching characteristics
6		X	US 6337269 B1	20020108	16	Method of fabricating a dual damascene structure

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
1	438/634	438/633; 438/687		Yuang, Yu-Shen	X				
2	438/638	438/687; 438/692		Bekiaris, Nikolaos et al.	X				
3	430/314	430/311; 430/313; 430/316; 430/317		Hsue, Chen-Chiu et al.	X				
4	438/624	257/750; 257/751; 257/760; 257/762; 438/627; 438/633; 438/634; 438/636; 438/637; 438/638; 438/687		Usami; Tatsuya	X				
5	430/313	216/16; 257/E21.579; 257/E23.019; 430/317; 438/629; 438/637; 438/638		Parikh; Suketu A. et al.	X				
6	438/618	438/623; 438/636; 438/637; 438/638; 438/640		Huang; I-Hsiung et al.	X				

DOCUMENT-IDENTIFIER: US 20030119307 A1

TITLE: Method of forming a dual damascene structure

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Abstract Paragraph - ABTX (1):

A method of forming a dual damascene structure on a substrate having a dielectric layer already formed thereon. In one embodiment the method includes depositing a first hard mask layer over the dielectric layer; depositing a second hard mask layer on the first hard mask layer; depositing a third hard mask layer on the second hard mask layer and completing formation of the dual damascene structure by etching a metal wiring pattern and a via pattern in the dielectric layer and filling the etched metal wiring pattern and via pattern with a conductive material. In one particular embodiment the second hard mask layer is an amorphous carbon layer and the third hard mask layer is a silicon-containing material.

Summary of Invention Paragraph - BSTX (20):

[0019] One embodiment of the of the method of the invention forms a dual damascene structure on a substrate having a dielectric layer formed thereon by depositing a first hard mask layer over the dielectric layer; depositing a second hard mask layer on the first hard mask layer; depositing a third hard mask layer on the second hard mask layer and completing formation of the dual damascene structure by etching a metal wiring pattern and a via pattern in the dielectric layer and filling the etched metal wiring pattern and via pattern with a conductive material.

Summary of Invention Paragraph - BSTX (21):

[0020] In some embodiments the second hard mask layer is an amorphous carbon layer and the third hard mask layer is a silicon-containing material. In one

particular embodiment where the dielectric layer is a porous low k silica film,
the amorphous carbon layer has a carbon content of between 40-90 percent, a
hydrogen content between 10-50 percent and a nitrogen content of between 0-10
percent. The relatively high carbon content enables the layer to have a high
etch selectivity with respect to the porous silica low k layer thereby enabling
the layer to be relatively thin. In other embodiments the third hard mask is a
silicon oxide, silicon nitride or silicon oxynitride film. The third hard mask
is used to protect the second hard mask during the stripping of an overlying
photoresist layer and/or organic antireflective coating. Silicon oxide,
silicon nitride and silicon oxynitride all exhibit a high etch selectivity to
standard oxygen-plasma photoresist stripping processes thus enabling the third
hard mask layer to be even thinner than the second hard mask layer. In one
embodiment, the combined thickness of the second and third hard mask layers is
no more than 1000 .ANG. with the third hard mask layer having a thickness of
400 .ANG. or less.

Summary of Invention Paragraph - BSTX (23):

[0022] According to another embodiment of the method of the invention, a
dual damascene structure is formed over a substrate having a first layer
interconnect layer already formed thereon, where the first interconnect layer
includes a dielectric material formed between a plurality of conductive lines.
The method of the embodiment forms a multilayer dielectric stack over the first
interconnect layer including a barrier dielectric layer, a via dielectric layer
and a porous low dielectric constant layer. A first hard mask is then formed
over the porous low dielectric constant layer, a second hard mask is formed
over the first hard mask and a third hard mask is formed over the second hard
mask. Next, an antireflective coating is formed over the third hard

mask and a
photoresist layer is formed over the antireflective coating. The photoresist
layer is then patterned in accordance with a metal wiring pattern to expose
selected portions of the antireflective coating, and the antireflective coating
and third hard mask layer are etched layer to transfer the metal wiring pattern
from the photoresist layer into those layers. The photoresist layer and
antireflective coating are stripped and the second hard mask layer is etched to
transfer the metal wiring pattern to the second hard mask layer. Next, a
second antireflective coating is deposited over the patterned second hard mask
layer and a second photoresist layer is formed over the second bottom
antireflective coating. The second photoresist layer is then patterned in
accordance with a via pattern to expose selected portions of the second
antireflective coating and a via hole is etched through the second
antireflective coating, the third, second and first hard mask layers and into
the porous low dielectric constant layer. The second photoresist layer and
second bottom antireflective coating are removed, and the metal wiring pattern
is etched into the porous low dielectric constant layer while the via pattern
is etched further into the dielectric stack. Next the barrier layer is etched
through in the via to expose portions of the conductive layer and the second
hard mask is removed. Finally, the etched via and metal wiring pattern are
filled with a conductive material and planarized.

Detail Description Paragraph - DETX (10):
[0037] Referring to FIG. 5c, a three layer hard mask structure 120 is formed
over dielectric layer 110 (step 162). Hard mask structure 120 includes a first
hard mask layer 122, a second hard mask layer 124 and a third hard mask layer
126. As already discussed, one important aspect of the present invention is
the different physical properties that each of layers 122, 124 and 126 exhibit

and the relationship between these properties and the etch chemistries used to subsequently pattern the layers and the underlying dielectric layer 110. In one embodiment, layer 122 is generally a nonporous, silicon-containing film. In some embodiments layer 122 is a BloK.TM. film. Such a film has a dielectric constant in the range of 4.0-5.0. It is generally desirable that the dielectric constant of layer 122 be relatively low since portions of layer 122 remain in the damascene structure after its completion (see FIG. 3, layer 86). Thus, in other embodiments layer 122 is a carbon-doped silica layer, such as a Black Diamond.TM. film, that has a dielectric constant of less than 3.0.

Detail Description Paragraph - DETX (24):

[0051] Because hard mask layer 124 is a non-silicon containing material with completely different etching characteristics than dielectric stack 110, layer 124 can be considerably thinner than a silicon-containing hard mask layer that may otherwise be used. Using a non-silicon material, such as amorphous carbon, as layer 124, however, requires the use of third hard mask layer 126 to protect layer 124 during removal of overlying photoresist layer 142 and organic antireflective coating 140. Amorphous carbon films have material properties very similar to organic photoresist and antireflective coatings and would thus exhibit a very low etch selectivity to the photoresist/antireflective coating stripping process. Silicon-containing materials such as silicon oxide, silicon nitride and silicon oxynitride, however, exhibit a very high etch selectivity to such stripping processes allowing hard mask layer 126 to be very thin. These attributes of layers 124 and 126 allow the combined thickness of the layers to be considerably thinner than the thickness of hard mask layer 22 described with respect to, one known prior art process in FIGS. 1a-1h as described in more detail below.

Claims Text - CLTX (2):
1. A method of forming a dual damascene structure on a substrate having a dielectric layer already formed thereon, said method comprising: depositing a first hard mask layer over the dielectric layer; depositing a second hard mask layer on the first hard mask layer, wherein said second hard mask layer is an amorphous carbon layer; depositing a third hard mask layer on the second hard mask layer, wherein said third hard mask layer is a silicon-containing material; and completing formation of the dual damascene structure by etching a metal wiring pattern and a via pattern in said dielectric layer and filling said etched metal wiring pattern and via pattern with a conductive material.

Claims Text - CLTX (9):
8. The method of claim 1 wherein said third hard mask layer is selected from the group consisting of silicon dioxide, silicon nitride and silicon oxynitride.

Claims Text - CLTX (11):
10. A method of forming a dual damascene structure on a substrate having a dielectric layer already formed thereon, said method comprising: depositing a first hard mask layer over the dielectric layer; depositing a second hard mask layer on the first hard mask layer, wherein said second hard mask layer exhibits a high etch selectivity with respect to said dielectric layer; depositing a third hard mask layer on the second hard mask layer; and completing formation of the dual damascene structure including etching a metal wiring pattern and a via pattern in said dielectric layer and depositing a conductive material in said etched metal wiring pattern and via pattern.

Claims Text - CLTX (17):
16. The method of claim 15 wherein said third hard mask layer is

selected
from the group consisting of silicon dioxide, silicon nitride and silicon
oxynitride.

Claims Text - CLTX (21):
20. A method of forming a dual damascene structure, said method comprising:
providing a substrate having a first interconnect layer formed thereon, said
first interconnect layer including a dielectric material formed between a
plurality of conductive lines; forming a barrier dielectric layer over said
first interconnect layer; forming a via dielectric layer over said barrier
dielectric layer; forming a porous low dielectric constant layer over said via
dielectric layer; depositing a first hard mask layer over said porous low
dielectric constant layer, wherein said first hard mask is a silicon-containing
material; depositing a second hard mask layer over said first hard mask layer,
wherein said second hard mask layer exhibits a high etch selectivity to said
via dielectric layer and said porous low k dielectric layer; depositing a
third hard mask layer over said second hard mask layer, wherein said third hard
mask layer is a silicon-containing material; forming a bottom antireflective
coating over said third hard mask; forming a photoresist layer over said third
hard mask layer; patterning said photoresist layer in accordance with a metal
wiring pattern to expose selected portions of said organic antireflective
coating; etching said organic antireflective layer and said third hard mask
layer to transfer said metal wiring pattern from said photoresist layer to said
organic antireflective coating and said third hard mask layer; etching said
second hard mask layer to transfer said metal wiring pattern to said second
hard mask layer and removing said photoresist and bottom antireflective layer;
forming a second organic antireflective coating over said patterned second hard

mask layer; forming a second photoresist layer over said second organic antireflective coating; patterning said second photoresist layer in accordance with a via pattern to expose selected portions of said second bottom antireflective coating; etching a via hole through said second organic antireflective coating, said third, second and first hard mask layer and at least into said porous low dielectric constant layer; removing said second photoresist layer and said second organic antireflective coating; etching said metal wiring pattern into said porous low dielectric constant layer and transfer said via pattern into said via dielectric layer; etching through said barrier dielectric layer in said via to expose portions of said first interconnect layer; and filling said etched via and metal wiring pattern with a conductive material.